$CuInSe_2$ Nanowires from Facile Chemical Transformation of In_2Se_3 and Their Integration in Single-Nanowire Devices

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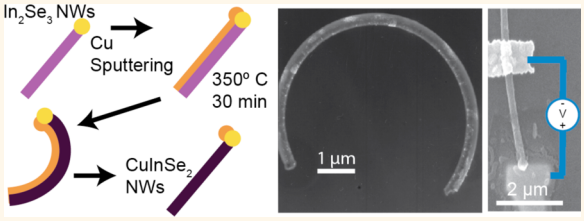
ABSTRACT Nanowire solar cells are receiving a significant amount of attention for their potential to improve light absorption and charge collection in photovoltaics. Single-nanowire solar cells offer the ability to investigate performance limits for macroscale devices, as well as the opportunity for in-depth structural characterization and property measurement in small working devices. Copper indium selenide (CIS) is a material uniquely suited to these investigations. Not only could nanowire solar cells of CIS perhaps allow efficient macroscale photovoltaics to be fabricated while reducing the amount of CIS required, important for a system with possible resource limitations, but it is also a photovoltaic material for which fundamental understanding has been elusive. We here present a recipe for a scaled up vapor liquid solid based synthesis of CIS nanowires, in-depth material and property correlation of single crystalline CIS nanowires, and the first report of a single CIS nanowire solar cell. The synthesis was accomplished by annealing copper-coated In_2Se_3 nanowires at a moderate temperature of 350 °C, leading to solid-state reaction forming CIS nanowires. These nanowires are p-type with a resitivity of 6.5 Ωcm. Evidence is observed for a strong diameter dependence on the nanowire transport properties. The single-nanowire solar cells have an open-circuit voltage of 500 mV and a short-circuit current of 2 pA under AM 1.5 illumination.



KEYWORDS: copper indium selenide · nanowires · photovoltaics · nanocharacterization · nanofabrication

The use of semiconductor nanowires (NW) as the active material in photovoltaic cells has received a great deal of attention in the last several years. There is hope that these new active materials will provide many benefits over current thin-film architectures by improving light management and charge collection,[1−5] as well as reducing processing costs by enabling improvements for low-cost substrates or materials.[1,6] In parallel with efforts to fabricate macroscale solar cells from large ensembles of nanowires, more fundamental work to understand the efficiency limits of nanowire photovoltaics has also been carried out, with the approach of fabricating and characterizing single-nanowire photovoltaic devices.[7] This has been successfully achieved in several material systems including silicon,[8,9] InP,[10] ZnO,[11] and Cu_2S,[12] among others. There is also a hope that one day small microfabricated devices may be powered by smaller photovoltaic elements,[13] and single-nanowire devices appear to be a prime candidate for this application. In order to achieve these goals, it will be necessary on one hand to choose materials systems most relevant to the photovoltaic application and on the other to maximize the performance of these tiny solar cells. We here present an investigation of single-nanowire photovoltaics in one of the most important thin-film photovoltaic material systems, copper indium diselenide, which until recently held the world record for thin-film performance of 20% for the closely related material copper indium gallium selenide (CIGS).[14] We report a scalable vapor liquid solid (VLS)-based synthesis for copper indium selenide (CIS) nanowires, provide detailed structural characterization of these materials, characterize the diameter dependence of their electrical behavior, and present the first report of a single-nanowire CIS solar cell.

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The fabrication of high-quality single crystalline CIS nanowires has been a significant research challenge. Previous work has focused on a variety of techniques, *e.g.*, electrodeposition into nanoscale anodic alumina oxide (AAO) templates,[15,16] the solution liquid solid technique,[17] the vapor liquid solid technique,[15,18] and the templated solid-state reaction (TSSR) in which single crystal In_2Se_3 nanowires are converted to CIS nanowires by means of solid-state reaction with copper.[19,20] The TSSR technique does produce apparently high-quality single crystal CIS nanowires, but until now the process has only been demonstrated on a single-nanowire basis. In previous work, electron beam lithography (EBL) was used to place a single copper pad on one end of an In_2Se_3 nanowire; then the transformation to CIS was accomplished by heating the wire to between 300 and 585 °C. In the current work, the insights gained during this study were used to scale the procedure up to converting an entire VLS batch of In_2Se_3 nanowires to CIS in a single annealing step, and the subsequent processing was developed to integrate these nanowires into single-nanowire solar cells.

RESULTS AND DISCUSSION

The entire process is illustrated in Figure 1 A. In_2Se_3 nanowires were grown by the VLS technique as previously reported.[21] The substrates used were SiN_x-coated silicon chips, pretreated with a thin, 1−5 nm gold film deposited by e-beam evaporation, which served as the source of gold catalyst for the VLS process. These In_2Se_3 nanowires on their growth substrate were then coated by dc sputtering with a 70−100 nm film of Cu, with thickness chosen to provide a large excess of Cu to the In_2Se_3 nanowires, considering the average In_2Se_3 nanowire diameter and its projected area. These copper-coated wires are then annealed in a tube furnace at a pressure of approximately 10 mTorr and a temperature of 350 °C for 30 min. SEM images of the growth substrates with In_2Se_3 nanowires (Figure 1B) and after Cu deposition and annealing (Figure 1C) show that the overall nanowire morphology is preserved during the annealing step, but that after annealing many nanowires are curved (Figure 1D). After annealing, a significant amount of Cu is left on the nanowires, and in order to fabricate single-nanowire devices, it is necessary that this material be removed. A simple cleaning step of 60 min submersion in 3 M aqueous HCl is sufficient for this task (Figure 1E and Supplementary Figure 1).

In order to follow this process to ensure the desired single crystalline structure of the CIS was preserved, transmission electron microscopy (TEM) characterization was performed on nanowires removed from the growth substrate after each important processing step. Figure 2 shows the results of TEM characterization after Cu sputtering but before the vacuum annealing process. Figure 2A shows a scanning TEM (STEM) dark field image of a copper-coated In_2Se_3 nanowire with the

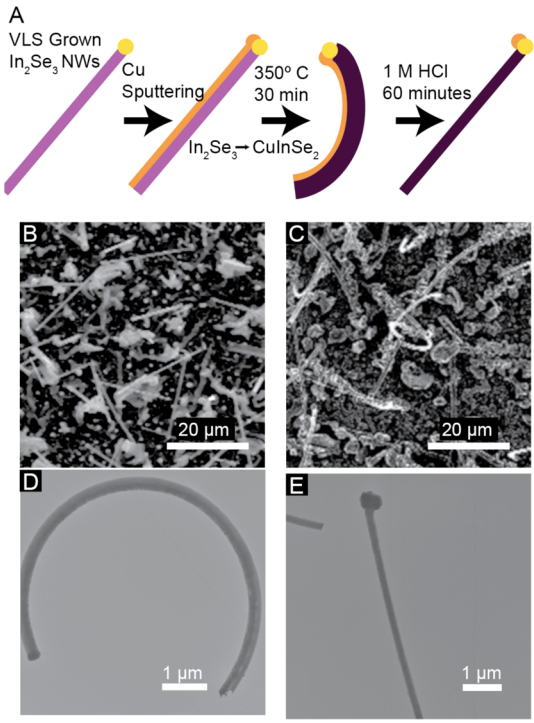

Figure 1. Synthesis scheme and results. (A) Four-step synthesis scheme for the production of single crystalline CIS nanowires. (B) SEM of In_2Se_3 nanowires after VLS growth. (C) SEM of nanowires after Cu sputtering and vacuum annealing. (D) Single Cu-coated CIS nanowire after annealing, showing a strong curvature. (E) Straight CIS nanowire after HCL cleaning.

dark gold catalyst particle on the end, although it is not possible in this image to resolve the difference between the In_2Se_3 and the Cu coating. TEM diffraction (Figure 2B) taken from the wire shows a pattern that can be primarily indexed to In_2Se_3, with several other scattered spots, which are diffraction from the polycrystalline Cu coating. STEM energy dispersive X-ray spectroscopy (EDS) analysis reveals the local composition. Figure 2C shows a higher magnification view of the nanowire near the catalyst particle, and Figure 2D shows EDS profiles taken along the red dotted line in Figure 2C. The Cu coating can now be clearly seen on the lower left side of the NW. Interestingly, there is a nonzero Cu signal from the entire width of the NW, indicating that during sputtering Cu atoms have enough energy to enter the In_2Se_3 crystal, either from substrate heating or simply due to the high energy of the impinging copper atoms. This is not extremely surprising, since previous work has shown that relatively low annealing temperatures can infiltrate some Cu into In_2Se_3,[19] although they are not sufficient to transform the crystal structure from hexagonal In_2Se_3 to chalcopyrite $CuInSe_2$. Panels E−H show two-dimensional EDS spectrum maps for Cu, In, Se, and Au. Again we see the nonzero copper signal from the entire NW, not just the coating, while In and Se are observed in the nanowire as well as one-half of the catalyst ball. The gold is

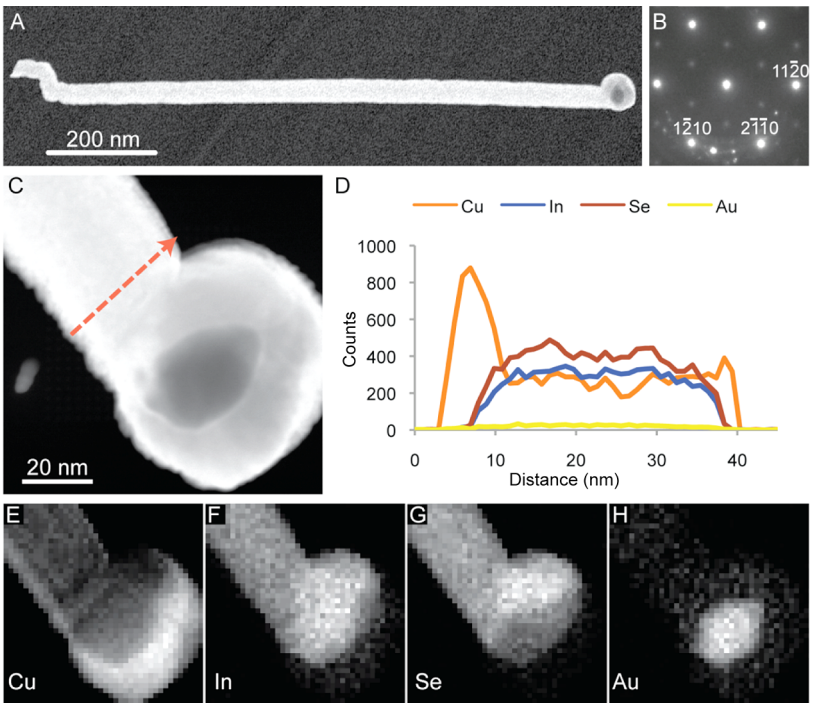

Figure 2. TEM analysis results for a Cu-coated In_2Se_3 NW before vacuum annealing. (A) Scanning transmission electron microscope dark field (STEM DF) image of an In_2Se_3 NW coated on one side with Cu by dc magnetron sputtering. (B) Diffraction pattern indexed to the In_2Se_3 hexagonal crystal structure, in the [0001] zone. (C) Higher magnification STEM DF image. The annotation indicates position of the energy dispersive spectroscopy (EDS) profile scan shown in D. (D) EDS profile scan showing counts along the line in C. (E–H) EDS spectrum maps showing the relative counts for each of the elements, Cu, In, Se, and Au.

contained only in the core of the catalyst, probably due to phase segregation in the cooling phase after the initial In_2Se_3 growth.

As seen in Figure 1D, after annealing many of the nanowires are curved. In order to understand the origin of the curvature, a detailed TEM investigation was performed (Figure 3). Figure 3A and 3B show bright field and dark field images of a curved NW. Diffraction along two different zones, the $\{-1-11\}$ and the $\{112\}$ in Figure 3C and D, demonstrates conclusively that the NW has transformed into the CIS structure after the annealing process. The diffraction in Figure 3C and D was taken with the smallest selected area electron diffraction (SAED) aperture positioned on the outside edge of the NW. The diffraction in Figure 3E was taken with a larger aperture, including diffraction features corresponding to both the CIS and the polycrystalline copper coating. Additional dark field TEM images formed with the Cu diffraction features show the material on the inside of the curve is polycrystalline Cu (Supplementary Figure 2).

Given that the CIS region is on the outside of the curve and Cu is on the inside, a simple explanation for the curvature can be proposed. The CIS lattice undergoes an approximately 6% expansion compared to In_2Se_3, and during annealing the Cu coating will contract as Cu atoms are dissolved into the CIS. Since the two films are bound at the interface, this expansion and contraction will lead to a strain that curves the entire structure. The fact that the CIS nanowire remains a coherent crystalline domain is illustrated in Figure 3B, D, and E. The diffraction patterns in Figure 3D and E are taken in the same diffraction zone, using two different selected area diffraction apertures at different positions, shown as the blue and red dotted circles in Figure 3B. It can be seen that a larger aperture, which includes a larger angle of curvature in the NW, spreads the spots seen in Figure 3D into streaks in Figure 3E. This indicates that the lattice itself is bent coherently along the arc of the nanowire. The dark field image provides more evidence for this. It was taken using the $\{112\}$ zone axis shown in Figure 3C, which shows diffracted beams at 60° intervals. The red dots in Figure 3B show a series of bright regions in the CIS portion of the nanowire, which correspond to these 60° increments. The CIS nanowire lights up as it rotates around the circle when it is aligned correctly for one of its diffracted beams to pass through the objective aperture used to form the dark field image. When the Cu is dissolved away by the HCl cleaning step, this strain is removed, as can be seen from TEM characterization for several etching times (Supplementary Figure 1), and the nanowires are left as single crystalline CIS nanowires in the chalcopyrite phase.

With the development of a larger scale technique for the synthesis of high-quality single crystalline CIS nanowires it becomes possible to have adequate samples for carrying out single-nanowire device

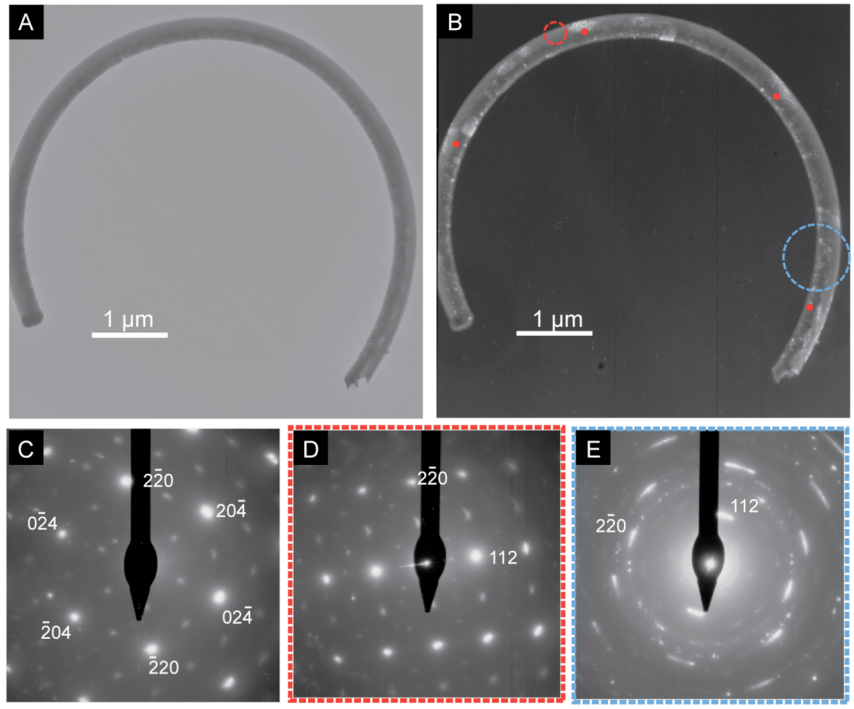

Figure 3. Transmission electron microscope (TEM) characterization of a CIS NW after conversion by vacuum annealing from a Cu-coated In_2Se_3 NW. (A) TEM bright field (BF) image, formed in the {112} zone. (B) TEM dark field (DF) image, formed in the {112} zone, selecting the [2−20] or [20−4] reflections. The dotted circles indicate the positions of the selected area electron diffraction (SAED) apertures used to form patterns D and E. (C) TEM diffraction, in the {112} zone. (D) TEM diffraction of the {−1−11} zone taken with the SAED aperture placed at the position of the red circle in B. (E) TEM diffraction in the {−1−11} zone taken with the larger SAED aperture placed at the position of the blue circle in B.

fabrication. The first step is to characterize the electrical behavior of the CIS nanowires, to understand any possible size effects on their transport properties, and to determine if they are p-type, as is desirable for the fabrication of single-nanowire solar cells. Figure 4 shows the results of electrical property characterization of single CIS nanowires. Devices were fabricated by dry transfer of CIS nanowires after annealing followed by the HCl cleaning step onto substrates prepatterned with large gold electrodes. EBL was used to define molybdenum contacts to the CIS nanowires. Figure 4C shows an SEM image of one such nanowire with four molybdenum contacts, and Figure 4A shows the results of two-point and four-point electrical measurements on this nanowire. It can be seen that the scans are nearly identical, indicating a very low contact resistance for the Mo contacts, which is to be expected from the use of Mo as the back contact in thin-film CIS solar cells. The two-point resistance is 342 MΩ, while the four-point resistance is 331 MΩ, indicating a contact resistance of 6 MΩ, or just 1.7% of the total two-point resistance. Similar results were found with many such devices. Resistance measurements were carried out for a large number of nanowires of different diameters, and the results of these measurements are shown in Figure 4D. It can be seen that the resistance of the nanowires increases dramatically for wires with a radius below 50 nm.

In order to assess the carrier type and estimate the mobility, a simple back gate transconductance method was used. The current is measured as a function of the gate voltage for a constant source drain voltage. The method relies on the movement of the bands in the device relative to the Fermi levels of the metal contacts. The sign of the transconductance is determined by the carrier type. If the conductivity increases with gate voltage, the material is n-type; if it decreases with gate voltage, it is p-type. Figure 4B shows this measurement for the two inner contacts of the nanowire, and the slope is clearly negative, indicating a p-type nanowire as desired. The transconductance can also be used to estimate the mobility,[22] according to the formula

$$\frac{dI}{dV} = \mu \frac{C}{L^2} V_d$$

where dI/dV is the transconductance, μ is the mobility, C is the capacitance, L is the channel length, and V_d is the source drain voltage. It is necessary to estimate the capacitance in order to do the calculation, and this can be difficult; however one can approximately use the capacitance of a finite cylinder separated by a dielectric from an infinite plane. This is only valid when the distance between the contacts is fairly large. The results of this calculation are shown in Figure 4E, and it can also be seen that the mobility appears to rapidly decrease for nanowires below 50 nm.

Assessing the exact origin of the diameter dependence of the nanowires' electrical properties will be

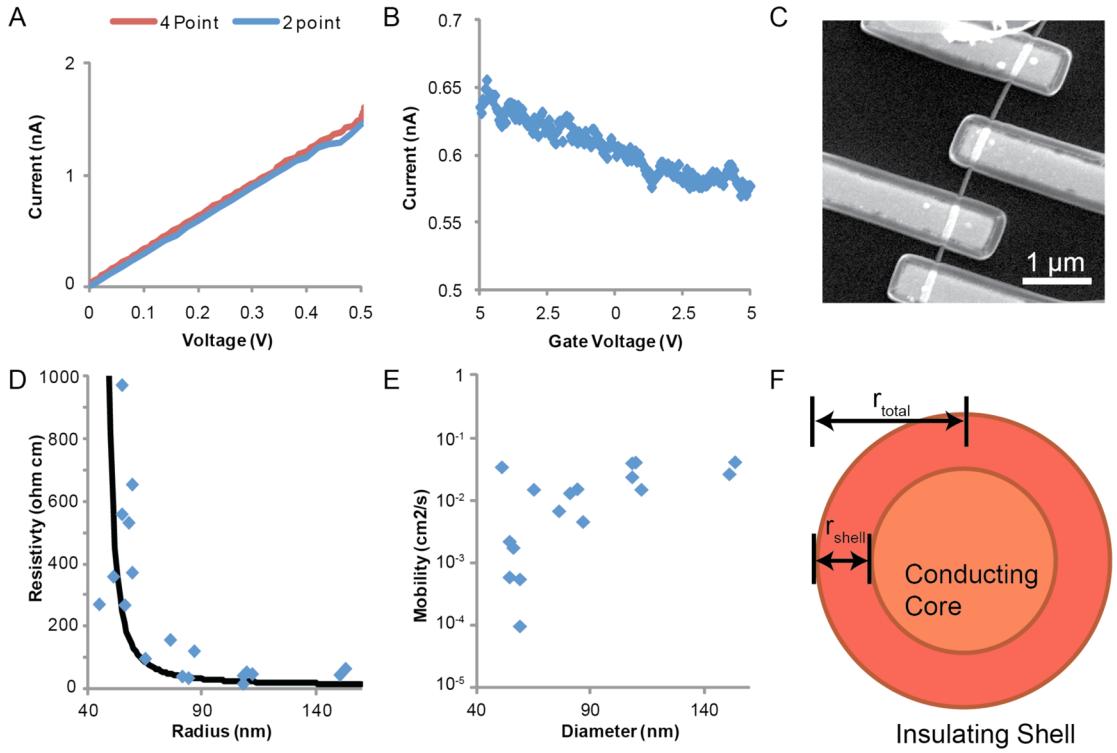

Figure 4. Electrical characterization of CIS nanowires. (A) Two- and four-point *I*–*V* measurements of the NW shown in C. (B) Transconductance measurement of the same NW. (C) SEM image of the NW measured in parts A and B. (D) Apparent total resistivity of many nanowires as a function of radius. The blue dots are the experimental data, and the black line is a model fit. (E) Mobility estimated from the transconducance measurements for nanowires as a function of radius. (F) Schematic of the proposed model.

very complicated, but a very simple model gives surprisingly good agreement with the data. It is well known that the electrical properties of the internal interfaces of CIS may differ from bulk properties, although the origin and nature of this difference is a topic of considerable debate.[23,24] This knowledge may be used for a very simple geometrical argument for the origin of the observed behavior. Suppose the core of the nanowire is relatively conductive p-type CIS, as hoped, and there is a uniform layer of more resistive material on the outside. For simplicity, let us assume this layer of material is, at least compared to the core, not at all conductive. As the total radius of the nanowire decreases, the conductive core will be pinched off, with the total resistance of the device following the simple relation

$$R = \frac{\rho_{core} L}{A_{core}} = \frac{\rho_{core} L}{\pi r_{core}^2} = \frac{\rho_{core} L}{\pi (r_{total} - r_{shell})^2}$$

where R is the total resistance, ρ_{core} is the resistivity, A_{core} is the cross sectional area of the core region, L is the device length, and r_{total} and r_{shell} are the relative radii of the total nanowire and shell, respectively. If we fit this to the observed data, using as a parameter only the thickness of the insulating shell and the resistivity of the conducting core, the black line shown in Figure 4D is the result. This fit yields parameters for the thickness of the insulating shell of 39 nm and the conductivity of the core of 6.5 Ωcm, which is reasonable for p-type CIS.

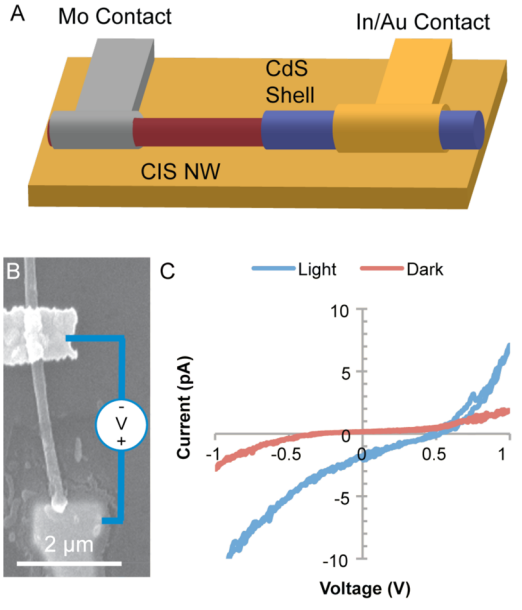

Figure 5. CIS single-nanowire solar cell schematic and measurement. (A) Schematic of the NW heterojunction structure, showing the CIS NW core, patterned CdS shell, and two metal contacts. (B) SEM image of such a device after fabrication. The CdS shell is too thin (~20 nm) to be easily observed in this image. (C) Light and dark *I*–*V* measurement for this device.

Although this simple model does not catch all the detailed physical parameters of the whole device, it is interesting how well it matches the observed trend.

It also gives an interesting length scale for the impact of the external surface on the nanowire electrical behavior, which may have important implications especially for current efforts to fabricate solar cells from very fine-grained nanocrystalline films.[25]

Having made CIS nanowires and demonstrated their p-type conductivity, it was possible to fabricate single-nanowire CIS solar cells. The schematic for these cells is shown in Figure 5A. The heterojunction was formed between the p-type CIS nanowire and a thin shell of n-type CdS grown by chemical bath deposition, which is the standard process used in CIS thin-film solar cells.[14] This process has been shown in previous work to grow a high-quality epitaxial shell of CdS on CIS nanowires, but there is a fairly narrow process window in which to deposit the CdS film, since at longer deposition times the nanoscale Kirkendall effect opens voids in the CIS nanowire cores.[18] Due to the epitaxial nature of the growth process, it is likely that the interface is clean and without interfacial oxide. This leads to the growth of a CdS film somewhat thinner than is typically used in thin-film cells, of only around 20 nm. This process can be patterned by EBL, allowing a thin film of CdS to be grown only over a segment of the CIS nanowire. An SEM image and light and dark *I*–*V* curves of the CIS nanowire solar cell are shown in Figure 5. The bottom, darker contact is Mo, and the top contact is In/Au, which is known to make good contact to CdS, both defined by EBL and deposited with e-beam evaporation and dc sputtering, respectively. The open-circuit voltage of the device is around 500 mV, which is reasonable for CIS, and the short-circuit current is 2 pA, which while small is easily measurable. One reason for the very small current is the opacity of the In/Au contact, which shadows most of the heterojunction area defined on the nanowire. The fill factor is relatively small, around 25%, and this is due primarily to a small shunt resistance and large series resistance, which can be seen in the slope of the IV curve through the short-circuit current. This is probably due to the very thin CdS coating. It is difficult to assess the total efficiency of the device due to uncertainty about the effective absorbing area, but it is probably below 1%. There are many improvements that can be made to the device, and one of the most critical is finding a heterojunction material to replace CdS that does not produce Kirkendall voids in the CIS nanowire. Nonetheless, this is the first demonstration of a single-nanowire CIS solar cell.

CONCLUSIONS

The primary importance of these observations is that they demonstrate the excellent potential of single-nanowire CIS solar cells as model systems for in-depth material characterization using TEM, STEM, and EDS to get superb insight into the structure of these small-scale solar cells, combined with the ability to carry out electrical characterization of working heterojunction solar cells. Given the large amount of uncertainty that still surrounds the material science of thin-film CIS solar cells, this can be an invaluable tool to understand the impact of the complicated processing involved in fabricating high-efficiency photovoltaic devices, especially the structural and property role of Ga incorporation,[26] Na doping,[27] and composition grading.[28] All of the processing steps described in this paper can also be carried out on SiN_x TEM membranes, so unambiguous one-to-one correlation of the structure and performance of individual CIS solar cells is possible and will be the most fruitful future direction for this work.

As research into single-nanowire photovoltaics progresses, it is also possible that direct applications may be found, perhaps in the area of small self-powering sensors or machines. So far, these CIS NW solar cells have not met the efficiencies demonstrated in single-NW silicon devices;[7] however fundamentally they should be attractive candidates. For very small solar cells, with maximum dimensions below several hundred nanometers, light absorption is a serious challenge. CIS is among the most highly absorptive materials known, so in principle a high-quality CIS solar cell should be able to be scaled to smaller sizes at reasonable efficiencies compared to an indirect band-gap material such as silicon. Future work will certainly lead to improvements in efficiency for these devices, and at these sizes their efficiency limits will be higher than for poorly absorbing materials.

METHODS

CIS Nanowire Synthesis. CIS nanowires were prepared by the template solid-state reaction technique, which has four steps. First In_2Se_3 nanowires were synthesized by the vapor liquid solid growth technique using solid In_2Se_3 (Sigma Aldrich) in the center area of a 2.5 cm diameter quartz tube furnace. The furnace temperature is set to 700 °C and pressure 15–50 mTorr. A carrier gas of 5% H_2/95% Ar is flowed through the tube at a rate of 120 sccm. In the downstream region of the furnace a temperature gradient exists, and silicon chips coated with 175 nm SiN_x and a 1–5 nm gold catalyst film approximately 1 cm × 1 cm are placed where the temperature is between 500 and 560 °C. A 30 min ramp from room temperature is followed by 4 h of NW growth, to obtain NWs with diameters ranging from 60 to 300 nm and lengths of 10's of μm. In the second TSSR step, these NWs are coated on the growth substrate with 70–100 nm of Cu by dc magnetron sputtering or e-beam evaporation. Third, the Cu-coated In_2Se_3 NWs are heated in a tube furnace at approximately 10 mTorr pressure to 350 °C for 1 h, and this converts them to curved, Cu-coated $CuInSe_2$ NWs in the chalcopyrite phase. Finally, the NWs are submerged in 1 M HCl for 1 h to remove the residual Cu. This step can be carried out on the growth substrate or after dry transfer to the device substrate.

Characterization. Scanning electron microscopy was carried out on an FEI Sirion scanning electron microscope with a field emission gun operated at 5 kV acceleration voltage. Transmission electron microscopy was carried out on an FEI Tecnai

transmission electron microscope with a field emission gun operated at 200 kV. Several modes were used, including standard TEM mode and scanning TEM mode. Composition analysis was carried out with an EDAX Genesis energy dispersive X-ray spectrometer. Line profiles and spectrum images were collected.

Electrical Device Fabrication. Electrical devices were fabricated by electron beam lithograpy using a modified FEI Sirion SEM operated at 30 kV with 20 pA current. Lithography was carried out on prepatterned substrates treated with CIS NWs by dry transfer. The HCl cleaning step was carried out before EBL on the device substrates. A double layer resist structure consisting of a P(MMA/MAA) EL 11 underlayer (Microchem) spun coat at 4000 rpm for 1 min and annealed at 160 °C for 1 min followed by a PMMA A6 top coat spun coat at 4000 rpm for 1 min and annealed at 180 °C. EBL patterned resist was used to define the Mo and In/Au contacts, which were deposited by dc sputtering and e-beam evaporation, respectively. EBL patterned resist was also used as a mask to define the CdS heterojunction in the CBD process. Electrical measurements were carried out with an Agilent B1500A parameter analyzer, and the solar spectrum used for the light curve in Figure 5 was collected with standard AM 1.5 illumination.

Chemical Bath Deposition (CBD) of CdS Heterojunction. CdS was deposited by CBD. The device substrate with EBL-defined resist mask was immersed in aqueous 1.5 mM $CdSO_4$ and 1.5 M NH_4OH in a 50 mL three-neck flask. The solution's temperature was quickly raised to between 60 and 70 °C. When the desired temperature was reached, 10 mL of aqueous 7.5 mM thiourea in 1.5 M NH_4OH was added to the flask, and the temperature held between 60 and 70 °C for between 5 and 16 min. A 20 nm shell, desired in this case, is obtained after approximately 5 min CBD time; however, the actual growth rate depends on several factors including the precise temperature as well as the pH of the growth solutions.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Additional TEM characterization of CIS NWs for two time points in the 1 M HCl cleaning step. Bright and dark field TEM highlighting the presence and location of polycrystalline Cu in the curved nanowire. This material is available free of charge via the Internet at http://pubs.acs.org.

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